Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Fourth Semester

Biomedical Engineering

BM3402- Analog and Digital Integrated Circuits

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	List out the ideal characteristics of an OP-AMP.	L1	1	2
2.	Why active guard drive is necessary in an instrumentation amplifier?	L1	1	2
3.	Define capture range and lock range of PLL.	L1	2	2
4.	Differentiate between conversion time and settling time.	L2	2	2
5.	Convert the given binary number to octal $(1010011.00101)_2$.	L2	3	2
6.	Subtract the given numbers using 2's complement method X=14, Y=10.	L2	3	2
7.	Interpret the logic equation for half adder.	L2	4	2
8.	What is priority encoder?	L1	4	2
9.	Define Flip flop.	L1	5	2
10.	What is shift register and list the types?	L1	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Interpret a differentiator using Op-Amp to differentiate an input signal with fmax = 150 Hz.	L2	1	16
			Or			
	b		Define Schmitt Trigger and explain about the working of inverting and non-inverting Schmitt trigger in detail.	L2	1	16
12.	a		With neat sketch explain the working principle of weighted resistor DAC using Op-Amp.	L2	2	16
			Or			
	b		Describe in detail about the Successive approximation ADC with neat sketch.	L2	2	16
13.	a	i	Inspect the switching function $f(w,x,y,z)=\sum m(0,1,3,4,12,14,15)$ with logic gates.	L4	3	8
		ii	Simplify the following expression y=m1+ m3+ m4+ m7+ m8+ m9+ m10+ m11+ m12+ m14 using K-map.	L4	3	8
			Or			
	b		Simplify the following Boolean expression in Sum of Product and Product of Sum using Karnaugh map and implement the same using logic gates. AC'+B'D+A'CD+ABCD.	L4	3	16

14.	a	Construct a full-adder circuit using two half-adders and an OR gate. Provide its truth table and logic diagram.	L3	4	16
		Or			
	b	Construct a 4-to-1 multiplexer using logic gates and draw its truth table. Explain its operation.	L3	4	16
15.	a	Develop a state table, characteristic table and an excitation table for SR Flip Flop.	L3	5	16
		Or			
	b	Discuss about the operation of 4-bit ring counter with waveforms.	L3	5	16